1. Introduction
Driven by the adoption of GPS functions, TV functions, MP3 music phones and video play-back needs in cell phone designs, more and more application-specific high speed switches are used widely for high speed data bus sharing or de-multiplexing with speed as high as 480Mbps for USB 2.0 signals. At the same time, integrated functions and analog features inside those switches become very attractive to designers to add value to their designs. In this article, some application examples for high speed analog switches in TV phone, GPS phone and dual camera phone designs even with USB charger detection are illustrated.

2. Quad High Speed Switches in TV Phones
With the fast adoption of CMMB in China mobile TV industry, the TV phone design is extremely popular in the market. Figure 1 is the typical design for TV phones with TV module and baseband sharing the reading or writing of the SD memory card. For effective high speed switching, a high bandwidth switch needs to be used for effective capacitance isolation. The open drain of the data bus now requires isolation of the pull-up resistor providing effective error-free communication. A dedicated high-speed clock path for each SDIO interface offers a flexible option for designers to use different clocks for different host, baseband processors or TV modules.
The bandwidth of the analog switch in both data and clock path has to be able to have -3db bandwidth of 150MHz at least under 30pf parasitic capacitance load. This allows effective passing of the high speed clock signals with minimal attenuation. >8KV I/O to ground ESD is typically needed for switch data port to allow customers to have flexibility to eliminate the external highly capacitive ESD diode if necessary. Figure 2 shows the similar SDIO application in GPS phone designs but here the switch (FSSD06) acts as the de-multiplexer to read and write the data between GPS module (SDIO devices) and SD card itself. In most applications, limited by the card type of either high voltage card (2.7 to 3.6V) or dual-voltage card (1.65-1.95V), there is a need for level shifting between the core processor I/O and peripheral devices with three power supplies that are needed for such switch devices with built-in bi-directional level shifting function for data bus and uni-directional level shifting for the clock data path.
3. High Speed USB 2.0 Switches in MP3 Phone Designs

Witnessed by end market demand, the MP3 player function has been widely adopted in most cell phone designs with high speed 2.0 (480 Mbps) capability for faster download and upload. In the same time, the charger through $V_{BUS}$ has been gradually adopted in China region driven by government USB charger standard. Charger detection becomes a key “must have” feature required by designers. Reliable charger detection is critical for “SHORT” connection detection between D+/D- pins in the all different application scenarios such as under data mode and non-data mode with system interference such as ground bounce and EMI noise interference. Figure 3 demonstrates such application with the high speed capable USB 2.0 switch integrated with charger detection function. The MP3 ASIC with high speed USB 2.0 capability can communicate effectively with the computer host for faster download or upload of music songs for MP3 playing. A high speed USB switch is needed here to isolate the full speed USB output port of the baseband processor with high output capacitance. The switch must be placed close to the USB controller output for minimal signal reflection.

In such applications, whenever the $V_{BUS}$ is plugged in with either charger or data cable, the switch needs to be enabled to be closed. The USB controller pull-ups the D+ line to initiate the talk to host through internal integrated 1.5 KOhm pull-up resistor. If D+ and D- is short together in standard charger case, then internal detection circuit will respond to such case to send out a FLAG signal to baseband GPIO input. In such application, the ON capacitance of the switch channel has to be low enough to allow the USB 2.0 signal pass through to be able to be compliant with USB 2.0 requirement. High ESD (>8KV I/O to ground) of the data port is important to offer the customer flexibility to move out the bulky ESD diode outside with high parasitic capacitance as well, which can slower down the edge rate being critical for eye compliance test for
4. High Speed Low Parasitic Capacitance Switches in Dual Camera Phone Designs

Driven by the 3G infrastructure and Olympic games in China, 3G is being launched gradually in key cities to support high speed multimedia audio/video stream upload and download. One of direct benefits end customers can get is the faster speed for video conference with dedicated camera in addition to the higher solution camera for personal picture. Those dual camera modules have to share the same data inputs at the base band side with different pixel clock and data streams. For higher resolution camera output, the pixel clock and data are high frequency TTL signals, which can have signal reflection risk causing the bit error rate if it shares the data bus with lower resolution camera module. This is even worse when the lower resolution camera module sits on the flip side of the slider phone or swivel phones. The long trace hanging over at the input of baseband processor will cause the reflection whenever under the high resolution camera mode since TTL line is un-terminated. The solution for such design challenge is to cut off the long and highly capacitive trace for low resolution camera under high resolution mode. This requires a switch along the low resolution camera data path with ultra low OFF capacitance to support 11 channel data including the data, clock and control signals. Figure 4 is a perfect solution for such applications with parasitic OFF capacitance as low as 2pf. This switch has to be placed close enough to the baseband’s input of lower resolution camera data inputs to eye opening.
effective cut off the parasitic capacitance of the long trace. In addition, the trace between high camera module to baseband processor needs to be minimized for lowest distortion of high speed pixel clock and data. Of course, low power consumption of the switch device is desirable as well for portable applications. 1uA power consumption is a key attractive feature for such switch products compared with active solution such as tri-state output buffer with much higher power consumption at mA grade.

Figure 4 Low OFF Capacitance Switches in Dual Camera Phone Designs

5. Summary
With the fast growing audio/video market in portable multimedia applications, application-specific high speed signal switch products will continue to offer a strong advantage in end designs to improved signal integrity allowing error free data transfer. Meanwhile, integrated application-specific features such as level shifting, charger detection or other low $I_{\text{CCT}}$ feature will help designers further reduce the BOM cost as well. This is highly desirable in main stream market such as low cost but rich feature phone designs in Asia.